Multi-Objective Design Automation for Microfluidic Capture Chips

Lisa Chen, William H. Grover, Manu Sridharan, *Member, IEEE,* and Philip Brisk, *Senior Member, IEEE*

***Abstract*—Microfluidic capture chips are useful for preparing or analyzing a wide range of different chemical, biological, and medical samples. A typical microfluidic capture chip contains features that capture certain targets (i.e. molecules, particles, cells) as they flow through the chip. However, creating optimal capture chip designs is difficult because of the inherent relationship between capture efficiency and flow resistance: as more capture features are added to the chip, the capture efficiency increases, but the additional features slow the flow of fluid through the chip. This paper introduces the use of multi-objective optimization to generate capture chip designs that balance the trade-off between maximizing target capture efficiency and minimizing resistance to fluid flow. Design automation for this important class of microfluidic chips has not been attempted previously. Our approach automatically produces a Pareto front of non-dominated chip designs in a reasonable amount of time, and most of these designs have comparable capture efficiency to hand-designed chips with far lower flow resistance. By choosing from the chip designs on the Pareto front, a user can obtain high capture efficiency without exceeding the flow resistance constraints of their application.**

***Index Terms*—Microfluidic Capture Chips, Design Space Exploration, Multi-objective Optimization**

I. Introduction

MICROFLUIDIC CHIPS have found important applications in a variety of fields, especially chemistry, biology, and healthcare. However, the process of designing a new microfluidic chip for a given application is slow, labor-intensive, and generally limited to researchers with expertise in the field. And while the design space of possible microfluidic devices is enormous, fabricating and testing each chip design is a laborious and time-consuming process. Consequently, most designers can only explore a handful of different device designs, and a researcher has no assurance that their final chip design is optimal or near-optimal for a particular purpose. Thus, there is a need to automate the process of generating new microfluidic chip designs for emerging applications.

This paper focuses on the algorithmic design of *microfluidic capture chips*, an important class of microfluidic chips. Such chips typically contain tiny features whose surfaces provide locations where molecules, particles, cells, and other targets of interest can be trapped as they flow in fluid through the chip. Many capture chips use arrays of small posts, or pillars, for this purpose [1]–[6]. For example, Sequist *et al*. [1] introduced a chip that utilized an staggered array of 78,000 μm-sized circular posts inside a microfluidic channel to capture circulating tumor cells (CTCs). This typical design is echoed in Figure 1a, in which fluid flows through a staggered array of circular posts inside a microfluidic channel. Previous work on design automation of microfluidic chips, summarized in Section VI, focused on chips with microvalves or performance-oriented metrics such as assay execution time without focusing on fluid physics [7]–[17]. This paper employs a methodological approach to microfluidic design automation, similar in principle to previous work designing passive microfluidic mixers [18], but with objectives and constraints relevant to analyte capture, rather than mixing.

At first glance, it might seem trivial to design the optimal microfluidic capture chip: simply pack as many capture features into the chip as possible. Indeed, this strategy would maximize the likelihood that a given target encounters a capture feature and is successfully trapped in the chip. But this approach has a fatal flaw: packing a microfluidic channel full of capture features would significantly slow or even block the flow of fluid through the channel (Figure 1b). Increasing the resistance to fluid flow likewise increases the amount of time and/or pressure required to pump a given volume of fluid through the capture chip, as the fluid-carrying capacity of a fluid channel is proportional to the *fourth power* of the channel's radius (assuming a circular-cross-section channel for simplicity). For comparison, the electrical-current-carrying capacity of a wire is proportional to the *second power* of the wire's radius (see Figure 2). For this reason, reducing the channel area available for fluid flow by packing the channel with capture features can have an *enormous* impact on the flow resistance of the channel, even more of an impact that our intuition from electronics might lead us to expect [19]. In other words, a chip with "perfect" capture efficiency may be practically useless if it takes hours or days (or dangerously high pressures) to pump a sample through it.

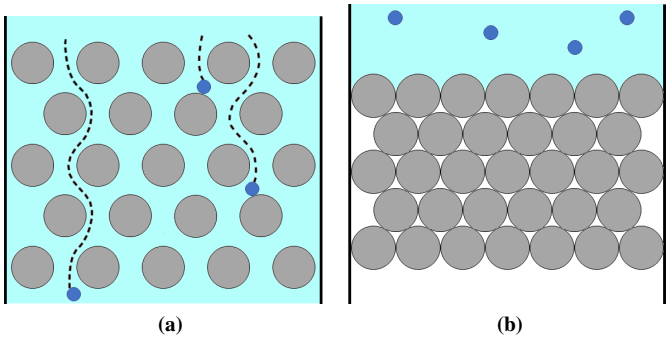
Conversely, it is trivial to reduce the flow resistance of a capture chip design—simply remove the capture features that are blocking the flow—but doing so will also reduce the capture efficiency of the device, possibly to the point that the device no longer serves its intended function.

Thus, *the ideal capture chip design for a given application must balance target capture efficiency and fluid flow resistance.* Balancing these two related, yet distinct, metrics within given specifications can be challenging, given existing arduous and time-consuming methodologies of designing, fabricating, and validating microfluidic chips by hand. We, therefore, aim

This work was supported by the National Science Foundation under grant numbers 1740052, 1910878, and 2019362.

L. Chen, M. Sridharan, and P. Brisk are with the Department of Computer Science and Engineering, University of California, Riverside, CA, 92521 USA e-mail: lchen314@ucr.edu; manu@cs.ucr.edu; philip@cs.ucr.edu.

W.H. Grover is with the Department of Bioengineering, University of California, Riverside, CA, 92521 USA e-mail: wgrover@engr.ucr.edu.



(a) **(b)**

Fig. 1: (a) A typical capture chip design consisting of a microfluidic channel filled with an array of circular posts. When a capture target (molecule, particle, cell, etc.) represented by a blue circle flows through the channel, it interacts with the posts and may eventually be captured by one. **(b)** When the channel is packed more densely with posts, the likelihood of a target interacting with a post and becoming trapped increases, but the paths for fluid to flow around the posts grow more narrow; this can severely limit or even stop the flow of fluid through the device and render it inoperable.

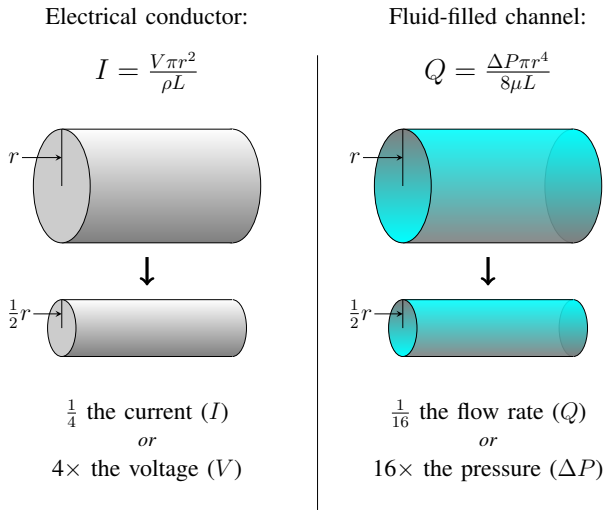


Fig. 2: Comparing the effects of size reduction on electronic and fluidic systems. For an **electrical conductor** (like a wire, or a trace in an integrated circuit), Ohm's Law and Pouillet's Law state that halving the radius r of the conductor causes the conductor to carry $\frac{1}{4}$ the current I (if the voltage applied V is unchanged) or require $4\times$ the voltage (if the current is to be unchanged). However, for a **fluid-filled channel** (like those in microfluidic devices), the Hagen-Poiseuille Law dictates that halving the radius of the channel causes the channel to carry $\frac{1}{16}$ the flow Q (if the pressure applied ΔP is unchanged) or require $16\times$ the pressure (if the flow rate is to be unchanged). This means that pressure and flow in a microfluidic device are far more sensitive to device design than voltage and current are in an electronic device. Consequently, just as voltage and current are essential aspects of electronic design optimization, pressure and flow *must* be included in microfluidic design optimization. (The other variables in the equations are constants: L = length of the conductor or channel, ρ = resistivity of the conductor, and μ = kinematic viscosity of the fluid.)

to improve the process through the use of design automation and simulations of capture chip designs, going beyond the regular arrays seen in Figure 1 to consider designs not obvious to human designers.

The objective of this paper is to algorithmically design microfluidic capture chips that balance the trade-off between target capture efficiency and fluid flow resistance. In doing so, this paper makes the following contributions:

- We characterize the design space for microfluidic capture chips in terms of the placement and geometry of capture features inside a microfluidic channel (Section II).
- We formulate the problem of microfluidic capture chip design as a multi-objective optimization problem (Section III).
- We non-exhaustively explore the design space for microfulidic capture chips using the Non-dominated Sorting Genetic Algorithm II (NSGA-II) [20] (Section III).
- We use finite element analysis simulation (*COMSOL Multiphysics*) to simulate both the capture efficiency and fluidic resistance of each design candidate (Section III).
- We report successful runs of automated capture chip design generation using a fixed and varying number of capture features and varying the feature geometries (Section V). Our key insights are:
  - Varying the number of posts yields comparable capture efficiencies to chips generated using a fixed number of posts, but with dramatically lower resistance to fluid flow; and
  - Circular-shaped posts tend to provide better overall performance in comparison to triangular, square, and pinwheel-shaped posts.

The paper is organized as follows. Section II defines the problem formulation for microfluidic capture chip design. Section III introduces our framework for microfluidic capture chip design, emphasizing the design space to explore, its encoding for evolutionary multi-objective optimization, and our approach to evaluate each chip design using finite element analysis simulation. Section IV summarizes the design of our experiments, including a number of relevant parameter settings and human-generated microfluidic chip designs that we use for comparison. Section V presents the results of our simulation experiments, leading to our conclusions outlined above. Section VI relates our technical contribution to similar attempts to apply the principles of electronic design automation to the domain of microfluidics. Lastly, Section VII concludes the paper and outlines new directions for future work.

II. Problem Formulation

We define a microfluidic capture chip as a microfluidic channel containing zero or more features that can capture a free-flowing target (molecule, particle, cell, and so on) if it contacts the features. Most published capture devices use circular posts arranged in regular arrays, not because these are necessarily optimal, but because they are simple to design. To

Fig. 3: The capture post shapes that are evaluated in this paper (left to right): circle, equilateral triangle, square, and pinwheel.

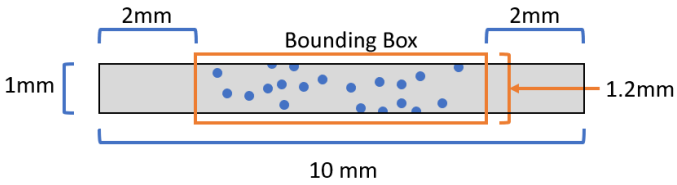


Fig. 4: Chip design constraints used in this study. Fluid flows from left to right through a section of channel that is 1 mm wide and 10 mm long. The bounding box designates the region of the channel where the algorithm can place posts (in this example, 0.2 mm diameter circular posts).

explore possible device designs that have not been considered before, we designed our framework to support multiple different post shapes (not just circles) and many different post arrangements (not just regular arrays). That being said, the range of possible capture chip designs is essentially infinite, so some design parameters must be constrained to make a study like ours feasible (for example, we did not consider chip designs that utilize two or more different post shapes in the same chip).

In this work, we constrain the design space to consider chips with four different post geometries shown in Figure 3: circular posts, square posts with a 0–90° rotation, equilateral triangle posts with a 0–360° rotation, and pinwheel-shaped posts with a 0–90° rotation. We also assume that all the posts in a given chip design have identical shapes and sizes; this is consistent with most published capture chip designs and allows us to have fewer changing variables and potentially faster convergence in our algorithm detailed later in Section III.

Figure 4 illustrates our assumptions about capture chip geometry and the restrictions that we impose on the design space. The designs are two-dimensional but are understood to represent a cross-section through a real three-dimensional channel (so, for example, each circular post actually represents a cylinder that spans from the floor to the ceiling of the channel). We assume that fluid flows from left to right through a 1-mm-wide channel; this channel width was chosen because it is representative of channel widths used in previous capture chips, wide enough to contain a reasonable number of capture posts and a reasonably high flow rate, and narrow enough that the flow inside the channel will be laminar (a Reynolds number $Re \ll 2300$ [21]; see Section III below for calculation details) as is typical in microfluidic chips. The total length of the channel is set to 10 mm; this value was chosen because the resulting channel is long enough to contain a large number of posts but short enough to be simulated using finite element analysis in a reasonable amount of time. The algorithm is free to place capture posts within a 6 mm $\times$ 1.2 mm bounding box in the center of the channel as shown in Figure 4. The 2-mm-long sections of channel immediately before and after the bounding box are intentionally left free of capture posts to provide room for the "entrance length" [21], the distance required for the fluid flow profile to fully develop and no longer be influenced by the inlet and outlet boundaries. The capture posts are free to overlap with each other (thereby forming larger capture features with more complex shapes) and overlap with the channel wall (thereby extending the walls or narrowing the fluid channel). Finally, while these design parameters were chosen for the reasons noted above and are representative of many existing microfluidic capture chips, these parameters can also be easily changed if a user wishes to optimize a chip design that cannot fit within the constraints used in this study.

We impose a maximum of N capture posts in our design and encode each post as a tuple $\alpha_i = (x_i, y_i, \theta_i, b_i), 1 \leq i \leq N$, where (x_i, y_i) is the coordinate of the post, $\theta_i \in \mathbb{R}$ is the rotational angle, and $b_i \in \{0, 1\}$ determines presence or absence of each post, i.e., setting b_i to 0 removes post α_i from the design. Chips with circular posts can omit θ_i, and the number of posts can be fixed by removing b_i and treating all posts as present.

We explored a range of values for the number of posts N. The specific post counts we used in the study were largely chosen arbitrarily, but we intentionally limited ourselves to 100 posts as a tradeoff between device complexity and simulation runtime:

- On one extreme, supporting devices with a massive number of posts (thousands or even millions) would be attractive because actual microfluidic capture devices sometimes use this many posts (e.g., [1]). However, performing finite-element simulation of these complex devices (the main time-consuming step in our technique) would take a prohibitively long amount of time.
- On the other extreme, simulating devices with only a handful of posts (say, 10 or fewer) would be attractive because these simulations can be performed quickly. However, having so few posts severely limits the range of possible device designs explored by our software and complicates comparisons with published results that use a larger number of posts.

In our experience, using 30 to 100 posts provided the needed "sweet spot" between device complexity and simulation runtime.

We characterize the performance of each microfluidic capture chip in terms of two objectives:

- **Capture efficiency**: the fraction of target molecules flowing into the chip that are successfully captured by the chip.
- **Inlet pressure**: the amount of pressure that develops at the inlet of the chip during operation (this is directly proportional to the flow resistance of the chip).

The next section formally defines these objectives.

III. Capture Chip Design Framework

Figure 5 depicts the key aspects of the microfluidic capture chip design framework presented in this section. The

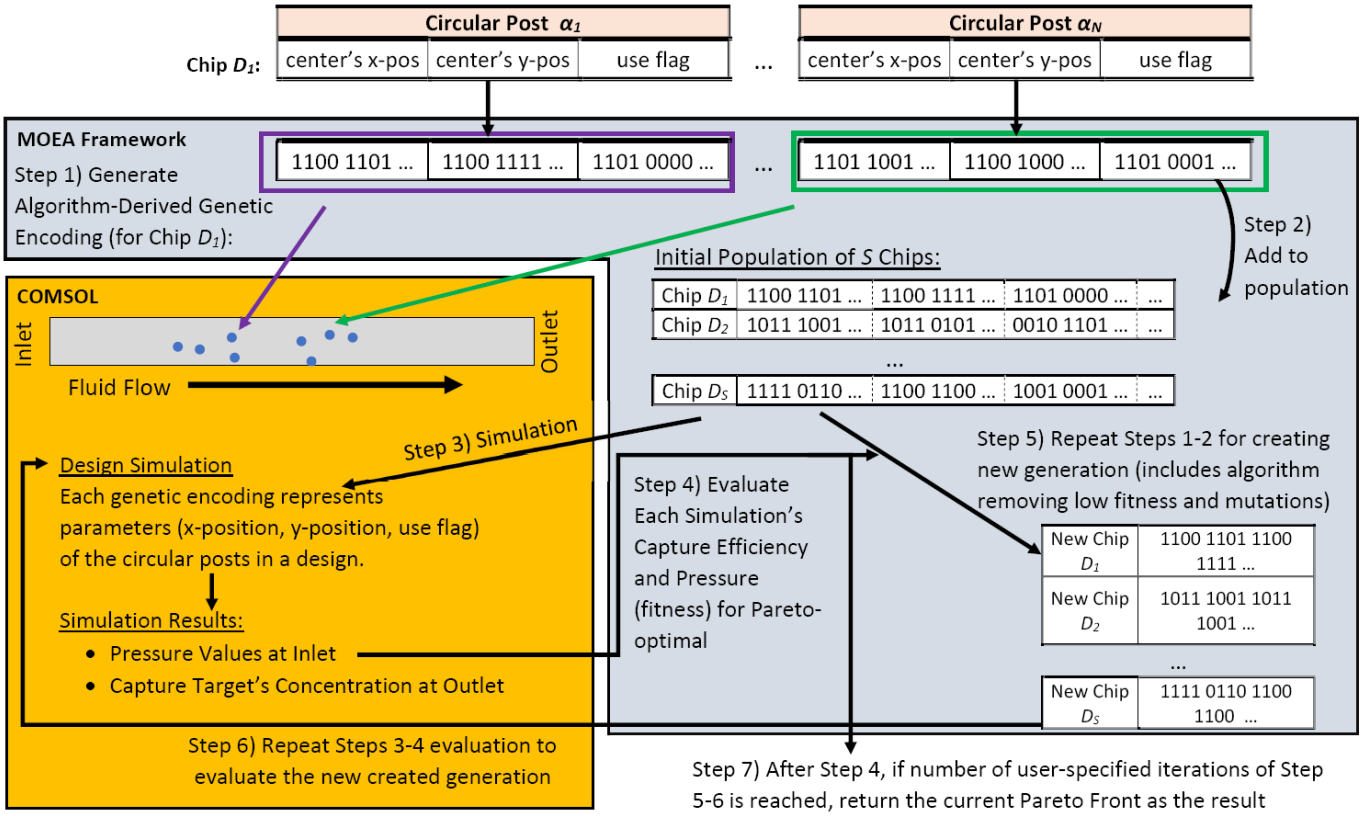


Fig. 5: Overview of our microfluidic capture chip design framework (configured for circular posts). The framework is implemented using NSGA-II, which is integrated into a larger open source Multi-Objective Evolutionary Algorithm (MOEA) framework [22], to enumerate chip designs and maintain a front of Pareto-optimal design points. NSGA-II/MOEA interfaces with finite-element simulation software (COMSOL Multiphysics) which performs the simulation. For each chip, the simulation predicts the concentration of the capture target at each point in the chip (used to quantify how much of the target was captured by the chip) and the pressure that develops at the inlet (which is an indicator of fluid flow resistance as discussed in Figure 2). NSGA-II maintains and evolves a population of encoded chip designs (chromosomes) which encode post positions (genes). Each chip design enumerated by the NSGA-II procedure is simulated by COMSOL Multiphysics, and the results are transmitted back to NSGA-II to update the Pareto Front based on fitness. This process repeats for a user-specified number of generations.

search is driven by NSGA-II [20], a multi-objective optimizer. NSGA-II encodes each chip design as a binary chromosome $D = \langle \alpha_1, \ldots, \alpha_N \rangle$, where $\alpha_i = (x_i, y_i, \theta_i, b_i)$ represents the position, rotation, and existence of the i^{th} post. NSGA-II maintains a population size of S chromosomes, $D_1, \ldots, D_S$.

During each generation, standard evolutionary procedures (see Figure 6) are applied to update the population. We applied uniform mutation and uniform crossover with mutation rates of $3/M$, where M is the number of variables in the chromosome.[1] Higher mutation rates increase population variability but tend to slow or otherwise limit the rate of convergence. The search terminates after a user-specified number of iterations.

We require at least 2 mm of spacing between the channel inlet and outlet and the center of each post; and we allow posts to intersect the channel walls as long as at least half of the post (e.g., determined by the radius r of a circular post) must reside within the channel:

$$x_c + 2 \leq x_i \leq x_c + L - 2 \tag{1}$$

$$y_c - r \leq y_i \leq y_c + W + r \tag{2}$$

Each chromosome D_j in the population is evaluated in terms of our two chosen objectives, capture efficiency E_j and inlet pressure P_j, denoted $(E_j, P_j) \leftarrow F(D_j)$, where F is the evaluation function. We implemented F using finite element simulation software (COMSOL Multiphysics) to estimate (E_j, P_j) for each design that NSGA-II enumerates. COMSOL multiphysics generates a mesh and computes the target concentration and pressure at each point in the mesh.

Capture efficiency (E_j) characterizes the anticipated percentage of the target flowing in the fluid that each chip design will capture. Let C_{inlet} be the concentration of target molecules at the channel inlet, and c_k, $1 \leq k \leq K$ be the capture efficiencies computed by COMSOL Multiphysics at

[1]To search for a chip design with N circular posts, the number of variables is $M = 3N$, as each tuple α_i has three fields, noting that θ_i is not needed; to search for a chip design with N square, triangular, or pinwheel-shaped posts, the number of variables is $M = 4N$.

all K mesh points on the channel outlet. We define the capture efficiency E_j of design D_j as follows:

$$E_j = \frac{\sum_{k=1}^{K} C_{inlet} - c_k}{K} * \frac{100}{C_{inlet}} \quad (3)$$

Inlet pressure (P_j) is reported in units of Pascals (Pa). In our simulations, we set the linear fluid flow rate at the inlet to 1 mm/s and sample the pressure at the central mesh point at the inlet. A flow rate of 1 mm/s was chosen because it is representative of the flow rates commonly encountered in microfluidic chips. Additionally, this flow rate will result in laminar (not turbulent) flow inside the chip. This can be verified by estimating the Reynolds number Re for our capture chip using the formula

$$Re = \frac{u\rho L}{\mu} \quad (4)$$

where u is the fluid flow speed (0.001 m/s), ρ is the density of the fluid (1000 kg/m^3 for water), L is the diameter of the microfluidic channel (0.001 m), and μ is the dynamic viscosity of the fluid (0.001 kg/(m·s) [21]. The result, $Re = 1$, is much less than 2300; this confirms that the flow inside our capture chip will be laminar, as is usually the case in microfluidics.

Just as the electrical resistance of a resistor determines the voltage drop, the fluidic resistance of the capture chip determines the pressure drop. A capture chip design with a high (or low) inlet pressure P_j therefore has high (or low) resistance to fluid flow.

In multi-objective optimization, it is rare to find one design point that is optimal among all objectives. Chip design (E_j, P_j) *dominates* solution (E_k, P_k) if

$$(E_j > E_k \wedge P_j \leq P_k) \vee (E_j \geq E_k \wedge P_j < P_k). \quad (5)$$

The Pareto Front of the search contains all chip designs enumerated by a run of NSGA-II that are not dominated by at least one other design. The user can then select any chip design from the Pareto Front based on her relative prioritization among the two objectives. This is not the Pareto Front for all possible capture chip designs, as the design space is too large to exhaustively enumerate.

IV. Experiment Design and Setup

We implemented our microfluidic capture chip design framework (Figure 5) using the COMSOL Multiphysics 5.5 and an open-source Java-based library that includes NSGA-II [22]. For each chip design enumerated by NSGA-II, we translated the design into COMSOL Multiphysics using its API to define shapes for the chip designs. We then simulated each chip design to obtain results for target capture and extracted the simulation result (E_j, P_j), which we then returned to NSGA-II for evaluation; NSGA-II determined if the new design dominated any designs in the current Pareto front, and updated the Pareto front accordingly.

Table I summarizes the chip geometry, COMSOL, and NSGA-II parameters that we used in our simulations. Our first set of experiments looked at the impact of various parameter settings on chip designs using circular posts. Our second set of experiments compared chip designs featuring circular to the non-circular post alternatives, using a slightly different combination of parameters.

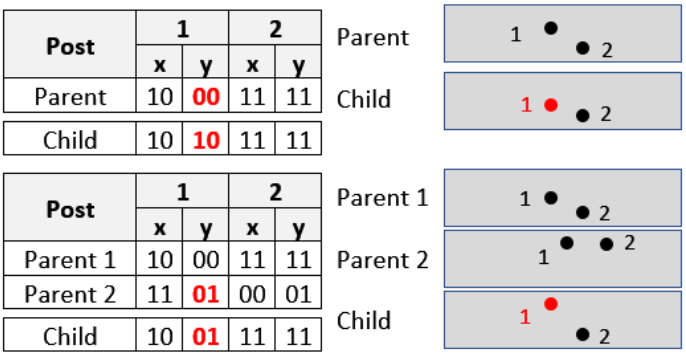


Fig. 6: A simplified example illustrating how uniform mutation (top) and uniform crossover (bottom) affect capture chip designs in our framework. Each variable is represented by a two-digit binary value (though in experiments, the binary values are much larger). For this example, we consider only the x and y coordinates of a circular post; to vary the number of posts (not shown), the Boolean flag for determining whether a post is used in the design will also have the same probability of being mutated as the x and y positions. For uniform mutation, each variable has an equal chance of being randomly mutated. For uniform crossover, each of the indices have equal probability of being swapped with another chip design of the same generation.

Table II summarizes the post geometries and parameters relating to rotation. Each pinwheel-shaped post consists of a small circle with four rectangular protrusions at 90° angles from one another. Square and triangular posts are rotated from their lower-left coordinate, while pinwheels are rotated from their center. Square and pinwheel posts rotate from 0-90° while triangular posts rotate from 0-360°.

All simulations were performed using an Intel Core i5-6600K CPU running at 3.50 GHz, with 32.0 GB RAM and running Windows 10 Education, OS Build 19042.985. We generated chip designs using exactly 31 posts, exactly 100 posts, and a variable number of posts ranging from 0-100. All chip geometry parameters, except for the number and position of posts, were kept constant. COMSOL failed to simulate approximately 5% of the chip designs that we generated and yielded an error. When this occurred, we eschewed simulation and assigned a low fitness value. The computational overhead of dealing with these failures did not significantly impact the overall runtime.

A. NSGA-II Variable Encoding

Recall that each post is encoded as a tuple $\alpha_i = (x_i, y_i, \theta_i, b_i)$. We use `RealVariables` to represent real numbers for the (x_i, y_i) position of each post and the rotation θ_i for non-circular posts. The b_i flags are also encoded as `RealVariables` to meet uniformity constraints imposed by the NSGA-II implementation (i.e., it does not allow us to specify a tuple comprised of three `RealVariables` and a Boolean). We encoded b_i to be a `RealVariable` in the

TABLE I: Defined parameters for COMSOL and NGSA-II.

Chip Geometry Parameters	
Channel Width	1 mm
Channel Length	10 mm
Post Quantity (N)	$\{31, 100, 0 \leq N \leq 100\}$
COMSOL Settings	
Inlet Fluid Flow Rate	0.001 m/s
Inflow Concentration	1 mol/m^3
Mesh Element Size	"Fine"
Fluid Setting	"Water"
NSGA-II Parameters (circular Posts)	
Population Size (S)	$\{25, 50, 100\}$
Number of Generations (G)	$\{40, 50, 80\}$
Number of NSGA-II Variables (M)	$2N$: Fixed number of posts $3N$: Variable number of posts
Mutation Rates	Uniform mutation: $3/M$ Uniform crossover: $3/M$
NSGA-II Parameters (Non-circular Posts)	
Population Size (S)	$\{50\}$
Number of Generations (G)	$\{40, 80\}$
Number of NSGA-II Variables (M)	$4N$: Variable number of posts
Mutation Rates	Uniform mutation: $3/M$ Uniform crossover: $3/M$

TABLE II: Settings for post shapes for designs with variable post quantity. M is defined as the number of NSGA-II variables while N is defined as the post quantity.

Shape	Dimensions	Rotation Position	Rotation
Circle	0.1 mm radius	–	–
Square	0.2 mm length	Bottom-Left	0 - 90°
Equilateral Triangle	0.2 mm sides	Bottom-Left	0 - 360°
Pinwheel: - Circle - Rectangle	 0.05 mm radius 0.2 mm x 0.05 mm	Center	0 - 90°

range $[0, 1]$ and interpreted its value as 1 if $b_i \geq 0.5$ and 0 otherwise.

B. COMSOL Implementation Details

Our chosen performance metrics, capture efficiency and inlet pressure, cannot be computed analytically for typical chip designs, so we estimate their values via simulation. To simulate a capture chip proposed by NSGA-II, COMSOL Multiphysics first constructs the chip geometry from rectangular and circular shapes and the generates a mesh for simulation. The *Laminar Flow* and *Transport of a Diluted Species* modules were used to establish the inlet flow rate and inflow target concentration of each chip design. All channel walls and post boundaries were marked as locations for fast irreversible surface reactions (surfaces where target molecules can be captured from the fluid). The API was also used to set other simulation parameters, including the physical properties of the fluid (water) and the granularity of the mesh used in finite-element analysis (finer mesh sizes tend to increase the accuracy of the simulation at the cost of longer simulation times). Finally, the API was used to execute the simulation and return the results to NSGA-II.

C. Human-Generated Designs

The first two human-generated chips are 31-post designs, named "Dense" and "Sparse" respectively. The "Dense" design packs the 31 posts into a small area; this a common design choice that aims for high capture efficiency at the cost of high resistance to fluid flow. The "Sparse" design spreads the posts out; this reduces the fluid flow resistance but also reduces the capture efficiency of the design. Finally, the third human-generated chip extends the "Dense" post spacing to fill the entire channel (101 posts); this design represents an attempt at manually maximizing the capture efficiency.

V. Results

This section evaluates our capture chip design framework. The results demonstrate that our system can discover many non-obvious chip designs with a variety of trade-offs between capture efficiency and flow resistance, and that, for the most parts, circular posts perform better than the other three geometries that we considered.

A. Generating capture chips with constant numbers of posts

We first algorithmically generated capture chip designs with a constant number of posts (31 posts each) to mirror the number used in the human-generated design and explored different values of S (the population size) and G (the number of generations). The results shown in Figure 7 compare the capture chip designs generated using three NSGA-II configurations: 1) 1000 chip designs ($S = 25$, $G = 40$); 2) 2000 chip designs ($S = 25$, $G = 80$); and 3) 5000 chip designs ($S = 100$, $G = 50$). For each configuration, Figure 7 only reports the chip designs that were Pareto optimal with respect to those that were enumerated. For chip designs that prioritize minimizing flow resistance (inlet pressure) at the expense of decreased capture efficiency, all three experiments yielded comparable-quality designs (represented by the points in the lower-left region of Figure 7). However, for designs that prioritize maximizing capture efficiency at the expense of increased flow resistance, the different experiments yielded different results. Specifically, the experiment with the largest number of designs ($S = 100$ and $G = 50$) yielded chip designs with the same high capture efficiency as the other experiments, but with dramatically lower flow resistance. Between the 1000 chip designs and 2000 chip designs, the improvement is small for double the number of generations. This demonstrates that as the number of chips simulated increases (via increasing the population size and/or the number of generations), the quality of chip designs on the Pareto Front tends to improve, especially at higher capture efficiencies.

Figure 8 plots the entire Pareto Front for the 5000 chip design run ($S = 100$, $G = 50$; green points) along with all the non-Pareto-optimal designs with inlet pressures lower than 9 Pa (green points). Also plotted is the result from the human-generated "Sparse" design with the same number of posts (black point in Figure 8). The results show that while the human-generated design has a slightly higher capture efficiency than the computer-generated designs, the human-generated design has a *dramatically* higher flow resistance.

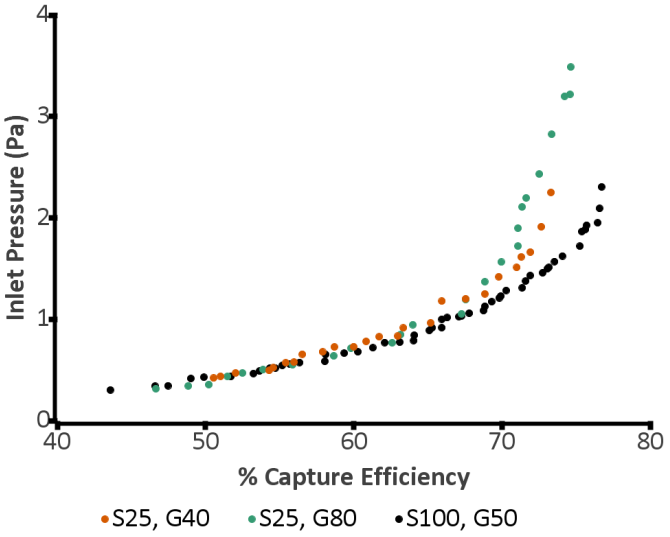


Fig. 7: Inlet pressure vs. capture efficiency for experiment runs with a constant number of posts (31) and different population sizes (S) and generation counts (G). The different experiments yielded similar results for designs that prioritize low flow resistance (lower-left corner). However, for designs that prioritize capture efficiency, the experiments with the largest total number of analyzed chips yielded the best designs (right side).

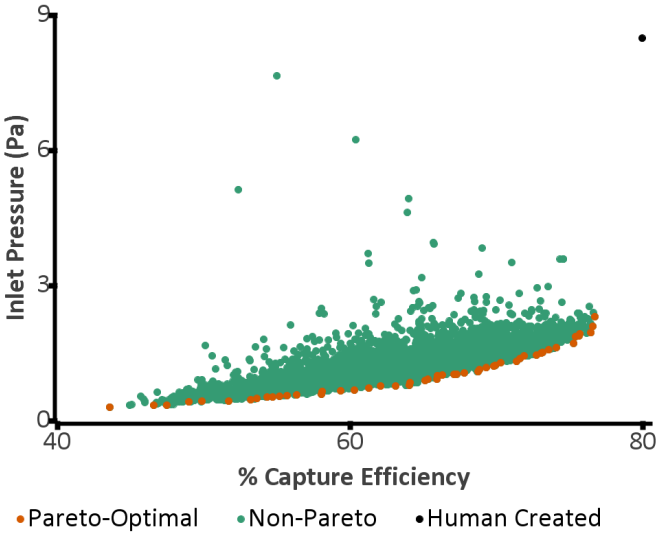


Fig. 8: Inlet pressure vs. capture efficiency for each capture chip design created during the experiment with 31 posts, population size $S = 100$, and generation count $G = 50$, along with the result from the human-designed "Sparse" chip design shown in Figure 9. Non-Pareto chip design results with inlet pressures higher than 9 Pa are not shown. While the human-designed chip has a slightly higher capture efficiency than our computer-designed chips, it suffers from significantly higher flow resistance.

Based on these results, if a researcher is willing to accept a modest (3 percentage point) reduction in capture efficiency, they can reduce their resistance to fluid flow by 73% by switching from the human-generated design to one of the Pareto-optimal designs generated by our framework. The actual chip designs and COMSOL simulation results for the designs with the highest capture efficiency from each of the three experiments (along with results from the human-created "Dense" and "Sparse" designs) are shown in Figure 9.

B. Generating capture chips with larger numbers of posts

Examination of the 31-post experiments in Figures 7–9 reveals that neither the computer-generated nor the human-generated designs had 100% capture efficiency. We hypothesized that the number of posts used in these experiments was too small for 100% capture efficiency, and more posts would be necessary for complete capture. To test this hypothesis, we performed an experiment using 100 posts (a 3× increase in the post count) with NSGA-II parameters $S = 50$ and $G = 40$ for a total of 2000 different designs.

The results from our 100-post experiment are shown in Figure 10. At first glance, these results look encouraging: the computer-generated results include designs on the Pareto-optimal front with 95% capture efficiency, which is higher than the 31-post designs. However, closer examination of Figure 10 shows that the flow resistance of the 100-post chips (up to 250 Pa) is *dramatically* higher than the 31-post chips (only up to 10 Pa, see Figure 8). And while the human-generated 101-post design does have near-100% capture efficiency, it also has around 5× higher flow resistance than the human-generated 31-post design described earlier. So while 100-post designs may be suitable for some applications that prioritize capture efficiency, their extremely high flow resistance makes them unsuitable for many other applications.

C. Generating capture chips with variable numbers of posts

The preceding experiments with 31- and 100-post capture chips show that the number of posts has a significant impact on capture chip performance: with too few posts the flow resistance is favorable but the capture efficiency decreases, and with too many posts the capture efficiency improves but the flow resistance suffers. Consequently, in subsequent experiments we decided to allow the algorithm to choose the number of posts up to a user-specified maximum.

In these experiments, the maximum number of posts was defined as 100 to align with the previous 100-post experiment, and tests were conducted with population size $S = 50$, and generation count $G = 40$ (2000 chips total) or $G = 80$ (4000 chips total). The plot of inlet pressure vs. capture efficiency for the $G = 80$ run is shown in Figure 11. Comparing these results with the previous 100-post results in Figure 10, we see that the designs with variable numbers of posts have comparable capture efficiencies but dramatically lower resistance to fluid flow. This combination is advantageous in most applications.

To understand why the variable-post designs had such low resistance to fluid flow, we examined the number of posts chosen by the algorithm in each of these designs. For all 4000 designs considered by the algorithm, the number of posts per design ranged from 29 to 65, with an average of 49 posts

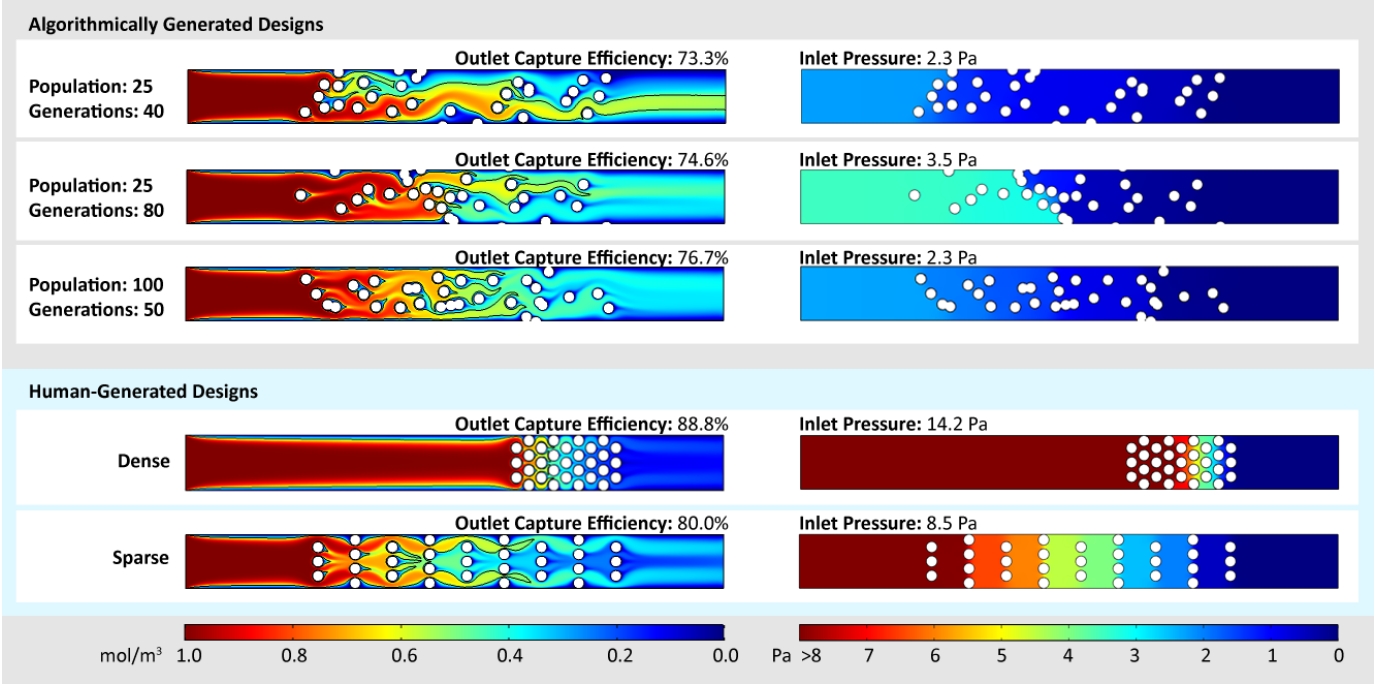


Fig. 9: Capture chip designs and simulation results for the designs with the highest capture efficiency from each of the three 31-post experiments, along with results from the human-generated "Dense" and "Sparse" chips. For each design, two simulation results are shown. **On the left** is the predicted concentration of capture target at each location of fluid in the chip during operation. All chips receive the same high concentration of target (red; 1 mol/m^3) flowing in from the left. As target is captured on the capture posts and channel walls, the concentration of target in the solution drops (indicated by a shift to orange, yellow, green, and blue). A chip with 100% capture efficiency would have no remaining target at the outlet (blue; 0 mol/m^3). **On the right** is the predicted pressure at each location of fluid in the chip during operation. All chips have atmospheric pressure (0 Pa) at the outlet on the right. Designs with high resistance to fluid flow develop high pressures (red colors) at the inlet on the left, and designs with low resistance to fluid flow develop low pressures (blue colors) at the inlet on the left. These results show that our computer-generated designs have comparable capture efficiencies to human-generated designs, but with dramatically lower resistance to fluid flow. This gives our computer-generated designs an advantage in many applications.

(Figure 12b). The results for the 47 Pareto-optimal designs were similar, ranging from 31 to 62 posts with an average of 48 posts (Figure 12c). With around half as many posts as the 100-post designs, the variable-post designs have lower resistance to fluid flow while still providing high capture efficiency.

The *shape* of the post-count distribution in our variable-post results also offers interesting insights into the algorithm's search for optimal designs. Since each device in the first generation has up to 100 posts but each post has a 50% probability of being present, the first generation has a normal (or Gaussian) distribution of post counts centered around 50 posts, as shown in Figure 12a). If the algorithm's design search was unguided, this symmetric distribution centered on 50 posts might be expected to endure in subsequent generations. However, that is not the case: Figure 12b shows that among all 4000 chip designs examined by the algorithm, the distribution of posts per design is asymmetric, with 59 being the most common number of posts. The extremes of the post count distribution are also different: on the high end, a sudden drop around 63 posts per design means that very few chips with more than 63 posts were considered by the algorithm; and on the low end, a longer and more gradual decline to 30 posts indicates the minimum number of posts considered by the algorithm. The distribution of Pareto-optimal post counts in Figure 12c shows that most optimal chip designs had either relatively large numbers of posts (54 to 62 posts per chip) or relatively small numbers of posts (31 to 40 posts per chip), and surprisingly few optimal designs had intermediate numbers of posts per chip. This almost-bimodal distribution of posts per chip in the Pareto-optimal designs could indicate that two different types of designs have emerged that are both optimal but use different numbers of posts, an idea we intend to explore in future work.

Figure 13 shows actual chip designs from the variable-post-count experiments. The design with the highest capture efficiency was obtained using a population size $S = 50$ and generation count $G = 80$; it has a capture efficiency of 89.3%, which is only 10 percentage points lower than the human-generated design that uses *nearly twice as many posts*. Additionally, the human-generated design has *over six times* the inlet pressure of our computer-generated design. This combination of very high capture efficiency with very low flow resistance means that our computer-generated designs can outperform human-generated designs in many applications.

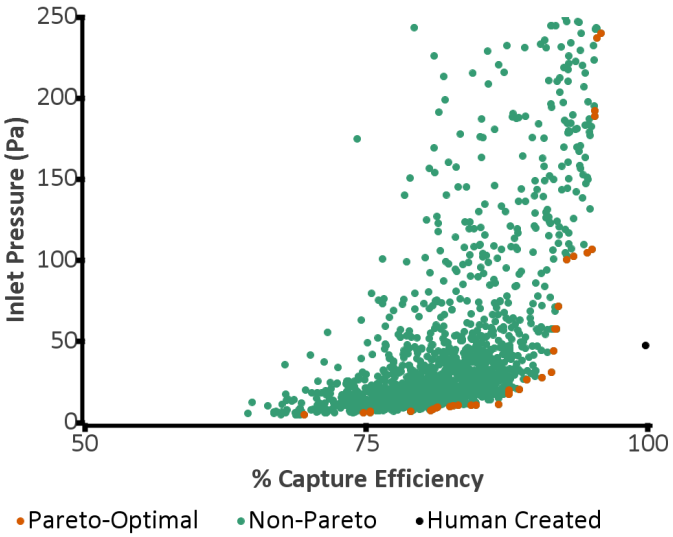


Fig. 10: Inlet pressure vs. capture efficiency for each capture chip design created during the experiment with 100 posts, population size $S = 50$, and generation count $G = 40$, along with the result from the human-designed 101-post chip shown in Figure 13. Non-Pareto chip design results with inlet pressures higher than 250 Pa are not shown. The results show that most of these 100-post designs have *extremely* high resistance to fluid flow (100x higher than the 31-post designs shown in Figures 7–9); this renders these designs unsuitable for many applications and suggests that an optimal post count for this device size lies between 31 and 100.

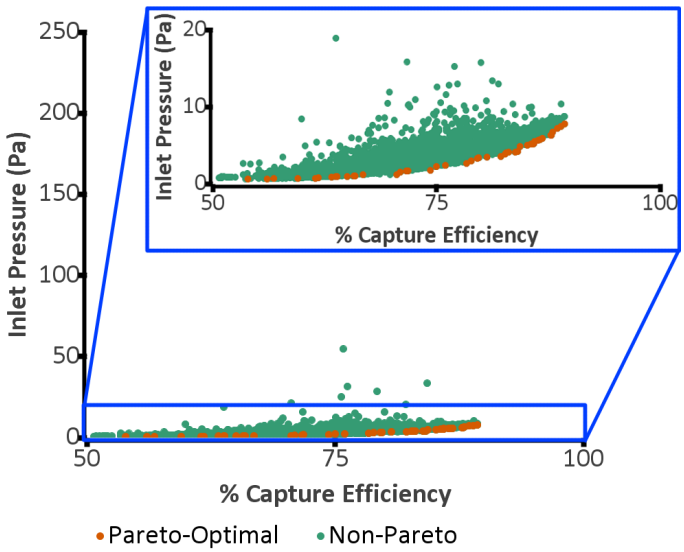


Fig. 11: Inlet pressure vs. capture efficiency for capture chip designs created using a variable number of posts (up to 100), with population size $S = 50$ and generation count $G = 80$. The axes are identical to Figure 10 for side-to-side comparison and 0-20 Pa data magnified for better visualization. Comparing this result to the constant 100-post results shows that allowing variable numbers of posts dramatically decreases the flow resistance of the resulting designs, with only a minimal decrease in maximum observed capture efficiency.

D. Generating capture chips with different shaped posts

The previous experiments exclusively considered microfluidic capture chips with circular post geometries; the set of experiments reported here serves to confirm the choice of circular posts compared to posts having square, triangular, and pinwheel-shaped geometries. It is worth noting that circular, square, and triangular posts are convex, while pinwheel-shaped posts feature multiple cavities. All experiments reported here were performed using a variable number of 0-100 posts, as this setting performed better than fixing the number of posts in our previous experiments. We performed two different runs: one where we generated 2000 chip designs ($S = 50$, $G = 40$) and another where we generated 4000 chip designs ($S = 50$, $G = 80$).

Figure 14 reports the results of these experiments. For the most part, circular posts performed better than the other shapes, both in terms of having lower inlet pressure and higher capture efficiency; square and pinwheel-shaped posts were able to attain 100% capture efficiency with the given settings, but the inlet pressures attained by these designs were extremely high in comparison and are likely to be impractical for use.

Triangles had the closest overall performance to circular posts, and in some cases, had lower inlet pressures toward the low-range of the capture efficiency spectrum. We thought that this may be an artifact of different mutation rates ($3/3N$ for circular posts; $3/4N$ for triangular posts), and wanted to verify that the circular posts were not benefiting from a higher mutation rate. We generated an additional 4000 triangular post chip designs using the higher $3/3N$ mutation rate, and included this run in Figure 14b. While this run did achieve higher capture efficiencies at some of the lowest inlet pressures, altogether, the chip designs featuring circular posts performed the best. Triangles were also retested using the higher mutation run, but the results uniformly fell short of the performance achieved by the circular designs (not shown in Figure 14).

E. Runtime analysis

Table III summarizes the runtimes for our optimization process for the circular post experiments described in the preceding subsections. As noted in Table I, various NSGA-II settings were used for the population size and number of generations. Increasing the number of generations in tandem with population size could potentially lead to an improved Pareto Front, at the cost of a longer search. In practice, a user can choose parameters that balance available computational resources with desired device performance. For our experiments, we observed the point at which improvements to the Pareto Front seemed to plateau, and set the number of generations accordingly. Most of the execution time during search is spent running chip design simulations in COMSOL Multiphysics. Finally, it is important to recognize that *all of these runtimes are inconsequential compared to the amount of time that would be required to manually fabricate and test such all of the chip designs that were explored.*

TABLE III: Runtime Summary for Circular Post Designs

Posts Qty	Population Size	Generations	Total Runtime (hr)	COMSOL Runtime (hr)	Average Time per Chip (s)	NSGA-II Runtime (s)
31	25	40	5.26	5.25	18.91	13.61
31	25	80	14.37	14.37	27.66	3.16
31	100	50	37.56	37.55	27.03	6.66
100	50	40	18.28	18.25	32.84	33.01
≤ 100	50	40	12.96	12.95	23.31	30.92
≤ 100	50	80	26.47	26.44	23.80	57.53

TABLE IV: Runtime Summary for ≤ 100 Posts for Different Shapes

Shape	Population Size	Generations	Total Runtime (hr)	Average Time per Chip (s)	Error %
Circle	50	40	12.96	23.31	5.20%
Triangle	50	40	21.48	38.64	1.30%
Square	50	40	27.20	48.92	4.15%
Pinwheel	50	40	37.16	66.78	3.15%
Circle	50	80	26.47	23.80	4.65%
Triangle	50	80	52.49	47.20	1.25%
Square	50	80	57.08	51.34	1.88%
Pinwheel	50	80	68.82	61.88	2.40%

Table IV summarizes the runtimes for the different post shapes we used in our designs as described in Section V-D. The post shapes have increasing simulation times in this following order: circles, triangles, squares, and pinwheels. This further shows that circular posts perform better as they are able to attain similar or better results in less time than the other shapes. This table also shows that all of the runs have lower error rates in the 4000 design run versus the 2000 design run. We found that COMSOL simulation errors are commonly caused by heavy overlapping of posts, causing errors in generating the mesh or contributing to COMSOL's inability to solve the simulation. Thus, this demonstrates that the algorithm with longer runs is more selective towards designs with less post overlap and less errors.

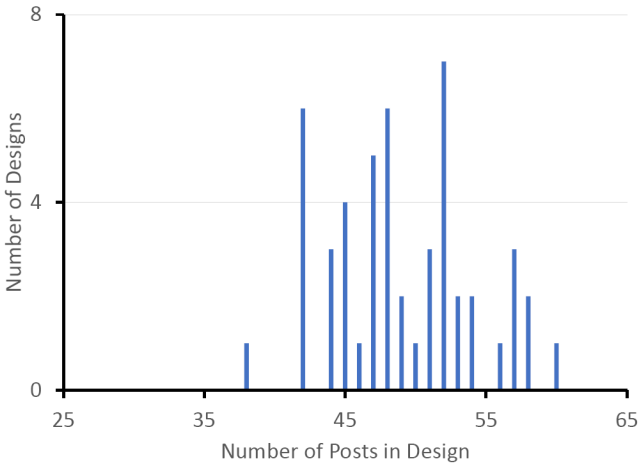
VI. Related Work

To the best of our knowledge, this paper represents the first effort to apply electronic design automation (EDA) principles to microfluidic capture chips. Prior work from our group took a similar methodological approach to the design of passive microfluidic mixers using NSGA-II as an optimizer and simulation by COMSOL to evaluate each candidate design choice [18]. The design space for passive microfluidic mixers considered circular posts exclusively in a much wider channel, and varied the position and radius of the posts. To optimize the analyze capture chips in this paper, we varied post geometries (circle, triangle, square, pinwheel) with rotations (exempting circular posts) and shifted their positions, but we did not vary the post dimensions (radius, length, width, etc.); additionally, in this work, it was necessary to mark channel walls and post boundaries as locations for fast irreversible surface reactions to simulate capture behavior, which was not needed in our prior work to simulate passive microfluidic mixers. The objectives were also different: while both optimizers account for inlet pressure/pressure drop as objectives, our prior work optimized a mixing score, whereas this work optimizing capture efficiency (Eq. 3). Somewhat more generally, the use of physical simulation to drive microfluidic EDA is an emerging trend: techniques that have been published to date include random enumeration of design points [23], multi-objective evolutionary algorithms [24], [25] (similar to both this work and Ref. [18]), as well as artificial neural networks and/or other machine learning-based approaches [26]–[28]. Notably, a recent review paper on machine learning for microfluidic chip design and control examined a wide variety of microfluidic designs applications, but did not mention any prior work on capture or post-based chips.

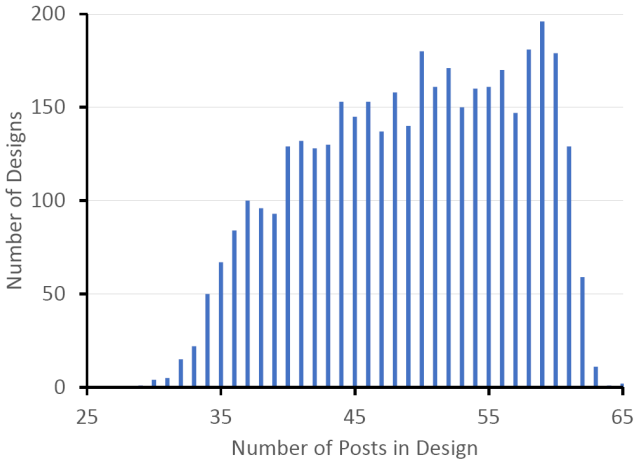
In this work we focused on pressure-driven fluid flow because it is arguably the most common method for driving flow in microfluidics, so our approach is widely applicable. There has been limited work on microfluidic design automation applied to device that utilize electrophoresis [29] or capillary flow [30]–[32] as driving forces. In general, our design optimization approach can utilize any driving force as long as the effects of that force can be accurately simulated (using e.g. a finite-element analysis tool like COMSOL Multiphysics as used in this work). So while we limited ourselves to pressure-driven flow in this work, our approach could be applied to designing microfluidic chips that utilize other driving forces, as long as those forces can be simulated on a computer.

A substantial number of design automation efforts in recent years have focused on channel-based microfluidic chips that feature integrated microvalves [7], [8], and optimize for performance-oriented metrics such as assay execution time or channel length [9]–[17]. These papers formulate the EDA problems to solve as optimization analogues of NP-complete decision problems with well-characterized discrete solution spaces that can be modeled, for example, using Integer Linear Programming (ILP). For the most part, these approaches do not consider the physics of fluid flowing inside channels, with or without obstacles such as posts, which are necessary in our case for particle capture. The simulation phenomena that drives our work cannot be captured as an ILP.

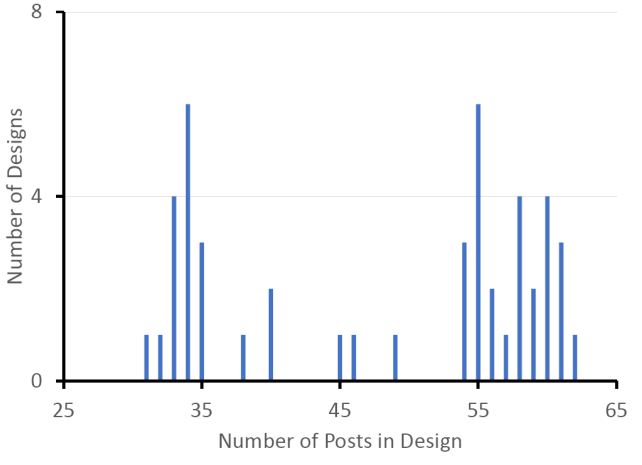
There has also been an abundance of work on applying EDA to electrowetting microfluidics, which transports discrete liquid droplets on 2D grid of electrodes [33], [34]. The discrete



(a) Initial Generation: 50 Designs



(b) All 4000 Designs



(c) All 47 Pareto-Optimal Designs

Fig. 12: Distribution of capture post counts in the designs from the variable-post-count experiment in Figure 11: **(a)** the initial generation with random numbers of posts per chip (50 chip designs), **(b)** all 4000 chip designs generated in the experiment, and **(c)** only the 47 Pareto-optimal chip designs from the experiment. The shapes of distributions (b) and (c) suggest that certain ranges of post counts per device are favored in optimal capture chip designs.

nature of the grid naturally lends itself to discrete optimization approaches; notably, there has been recent interest in simulating the underlying physics of the interal fluid flow within droplets, for example, to model the loss of droplet volume resulting from physical defects [35]. Despite the methodological similarity, this approach is at most tangentially related to this work due to the underlying technological dissimilarities.

Design automation methods for two-phase microfluidics [36]–[40], in which droplets are formed and merged inside of an immiscible carrier fluid, necessarily integrate physics models [41], [42]. Here, the objective is to passively route payload droplets in a fixed-geometry microfluidic channel network using the presence of control droplets whose contents do not directly take part in a chemical reaction [43]. Droplet routing is determined by the presence/absence of control droplets at specific designer-specified locations in the network. The objectives, constraints, and underlying physical models are quite different in comparison to the capture mechanisms that we consider here.

VII. Conclusion and Future Work

This paper has demonstrated the ability of multi-objective design automation mechanisms to create microfluidic capture chips with layouts that do not resemble human-generated designs. The key challenge is to find a good balance between capture efficiency and internal flow resistance (inlet pressure), which was overcome by permitting the optimizer vary the number of posts in the design. We also showed that circular posts perform better than square, triangular, and pinwheel-shaped posts, some of which are common in microfluidic chips. We anticipate that fabricated chips will minimally deviate from the simulation results, as we used mature and well-understood modules within COMSOL Multiphysics that have stood the test of time among microfluidics designers. Potential directions for future work are to extend the design space exploration to consider additional post geometries, non-rectangular channel dimensions, to consider other microfluidic chip functions beyond capture, to integrate active elements (e.g., pneumatically actuated pumps and valves) into the design, and to automatically design and evaluate larger-scale chips that integrate multiple laboratory functions.

References

[1] L. V. Sequist, S. Nagrath, M. Toner, D. A. Haber, and T. J. Lynch, "The CTC-Chip," *Journal of thoracic oncology : official publication of the International Association for the Study of Lung Cancer*, vol. 4, no. 3, pp. 281–283, Mar. 2009. [Online]. Available: https://www.ncbi.nlm.nih.gov/pmc/articles/PMC4486079/

[2] J. V. Green, D. Sun, A. Hafezi-Moghadam, K. Lashkari, and S. K. Murthy, "Microfluidic pillar array sandwich immunofluorescence assay for ocular diagnostics," *Biomedical Microdevices*, vol. 13, no. 3, pp. 573–583, Jun. 2011. [Online]. Available: http://link.springer.com/10.1007/s10544-011-9528-4

[3] L. Malic, X. Zhang, D. Brassard, L. Clime, J. Daoud, C. Luebbert, V. Barrere, A. Boutin, S. Bidawid, J. Farber, N. Corneau, and T. Veres, "Polymer-based microfluidic chip for rapid and efficient immunomagnetic capture and release of Listeria monocytogenes," *Lab on a Chip*, vol. 15, no. 20, pp. 3994–4007, 2015, publisher: Royal Society of Chemistry. [Online]. Available: https://pubs.rsc.org/en/content/articlelanding/2015/lc/c5lc00852b

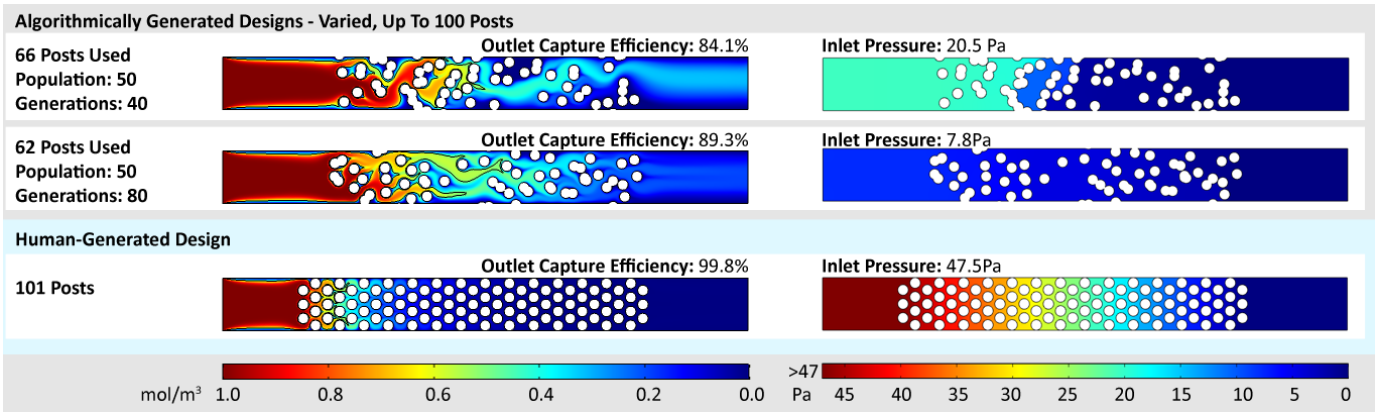


Fig. 13: Capture chip designs and simulation results for the designs with the highest capture efficiency from each of the experiments with variable numbers of posts, along with results from the human-generated design with 101 posts. Capture efficiency (left) and inlet pressure (right) are as described in Figure 9. These results show that our best computer-generated designs have comparable capture efficiency to the human-generated designs, but with *six times lower flow resistance* and *almost half the number of posts*.

[4] F. Fan, W.-H. Gu, X.-H. Wang, and S.-J. Chang, "Real-time quantitative terahertz microfluidic sensing based on photonic crystal pillar array," *Applied Physics Letters*, vol. 102, no. 12, p. 121113, Mar. 2013. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.4798836

[5] J. Hansson, H. Yasuga, T. Haraldsson, and W. van der Wijngaart, "Synthetic microfluidic paper: high surface area and high porosity polymer micropillar arrays," *Lab on a Chip*, vol. 16, no. 2, pp. 298–304, 2016. [Online]. Available: http://xlink.rsc.org/?DOI=C5LC01318F

[6] D. J. Howard, Y.-J. Seo, B. Hahm, and J. W. Kwon, "A Microfluidic Device With Concave Surfaced Micropost Array for Rare Cell Capture," *IEEE Sensors Journal*, vol. 14, no. 1, pp. 5–6, Jan. 2014, conference Name: IEEE Sensors Journal.

[7] M. A. Unger, H.-P. Chou, T. Thorsen, A. Scherer, and S. R. Quake, "Monolithic microfabricated valves and pumps by multilayer soft lithography," *Science*, vol. 288, no. 5463, pp. 113–116, 2000. [Online]. Available: https://science.sciencemag.org/content/288/5463/113

[8] W. H. Grover, A. M. Skelley, C. N. Liu, E. T. Lagally, and R. A. Mathies, "Monolithic membrane valves and diaphragm pumps for practical large-scale integration into glass microfluidic devices," *Sensors and Actuators B: Chemical*, vol. 89, no. 3, pp. 315–323, 2003. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0925400502004689

[9] W. H. Minhass, P. Pop, J. Madsen, and F. S. Blaga, "Architectural synthesis of flow-based microfluidic large-scale integration biochips," in *Proceedings of the 15th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, CASES 2012, part of the Eighth Embedded Systems Week, ESWeek 2012, Tampere, Finland, October 7-12, 2012*, A. Jerraya, L. P. Carloni, V. J. M. III, and R. M. Rabbah, Eds. ACM, 2012, pp. 181–190. [Online]. Available: https://doi.org/10.1145/2380403.2380437

[10] C. Lin, C. Liu, I. Chen, D. T. Lee, and T. Ho, "An efficient bi-criteria flow channel routing algorithm for flow-based microfluidic biochips," in *The 51st Annual Design Automation Conference 2014, DAC '14, San Francisco, CA, USA, June 1-5, 2014*. ACM, 2014, pp. 141:1–141:6. [Online]. Available: https://doi.org/10.1145/2593069.2593084

[11] K. Hu, T. A. Dinh, T. Ho, and K. Chakrabarty, "Control-layer routing and control-pin minimization for flow-based microfluidic biochips," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 36, no. 1, pp. 55–68, 2017. [Online]. Available: https://doi.org/10.1109/TCAD.2016.2568198

[12] W. H. Minhass, J. McDaniel, M. L. Raagaard, P. Brisk, P. Pop, and J. Madsen, "Scheduling and fluid routing for flow-based microfluidic laboratories-on-a-chip," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 37, no. 3, pp. 615–628, 2018. [Online]. Available: https://doi.org/10.1109/TCAD.2017.2729463

[13] T. Tseng, M. Li, D. N. Freitas, A. Mongersun, I. E. Araci, T. Ho, and U. Schlichtmann, "Columba S: a scalable co-layout design automation tool for microfluidic large-scale integration," in *Proceedings of the 55th Annual Design Automation Conference, DAC 2018, San Francisco, CA, USA, June 24-29, 2018*. ACM, 2018, pp. 163:1–163:6. [Online]. Available: https://doi.org/10.1145/3195970.3196011

[14] T. Tseng, M. Li, D. N. Freitas, T. McAuley, B. Li, T. Ho, I. E. Araci, and U. Schlichtmann, "Columba 2.0: A co-layout synthesis tool for continuous-flow microfluidic biochips," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 37, no. 8, pp. 1588–1601, 2018. [Online]. Available: https://doi.org/10.1109/TCAD.2017.2760628

[15] X. Huang, T. Ho, K. Chakrabarty, and W. Guo, "Timing-driven flow-channel network construction for continuous-flow microfluidic biochips," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 39, no. 6, pp. 1314–1327, 2020. [Online]. Available: https://doi.org/10.1109/TCAD.2019.2912936

[16] J. Weng, T. Ho, W. Ji, P. Liu, M. Bao, and H. Yao, "URBER: ultrafast rule-based escape routing method for large-scale sample delivery biochips," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 39, no. 1, pp. 157–170, 2020. [Online]. Available: https://doi.org/10.1109/TCAD.2018.2883908

[17] C. Liu, X. Huang, B. Li, H. Yao, P. Pop, T. Ho, and U. Schlichtmann, "DCSA: distributed channel-storage architecture for flow-based microfluidic biochips," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 40, no. 1, pp. 115–128, 2021. [Online]. Available: https://doi.org/10.1109/TCAD.2020.2994267

[18] J. Wang, N. Zhang, J. Chen, V. G. J. Rodgers, P. Brisk, and W. H. Grover, "Finding the optimal design of a passive microfluidic mixer," *Lab Chip*, vol. 19, pp. 3618–3627, 2019. [Online]. Available: http://dx.doi.org/10.1039/C9LC00546C

[19] F. A. Perdigones, A. Luque, and J. M. Quero, "Correspondence Between Electronics and Fluids in MEMS: Designing Microfluidic Systems Using Electronics," *IEEE Industrial Electronics Magazine*, vol. 8, no. 4, pp. 6–17, Dec. 2014, conference Name: IEEE Industrial Electronics Magazine.

[20] K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan, "A fast and elitist multiobjective genetic algorithm: NSGA-II," *IEEE Transactions on Evolutionary Computation*, vol. 6, no. 2, pp. 182–197, Apr. 2002.

[21] R. A. Granger, *Fluid Mechanics*, ser. Dover Books on Physics. New York: Dover Publications, 2012.

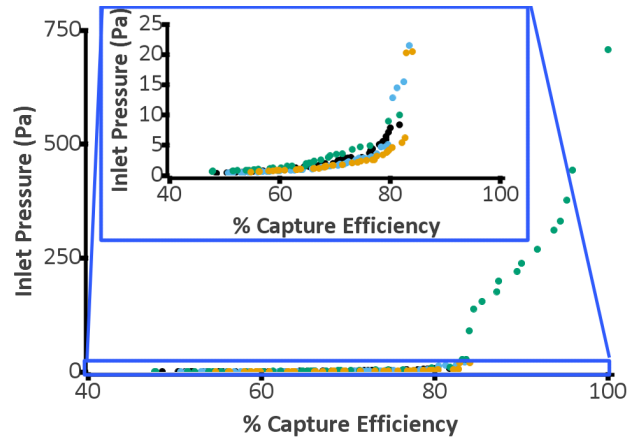
[22] "MOEA Framework, a Java library for multiobjective evolutionary algorithms." [Online]. Available: http://moeaframework.org/

[23] J. Wang, P. Brisk, and W. H. Grover, "Random design of microfluidics," *Lab Chip*, vol. 16, pp. 4212–4219, 2016. [Online]. Available: http://dx.doi.org/10.1039/C6LC00758A

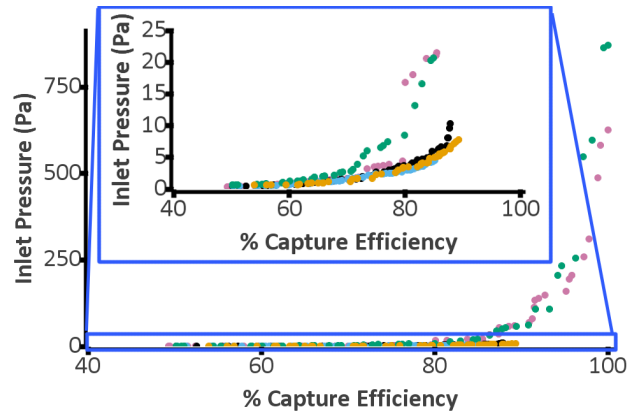
[24] D. Stoecklein, M. Davies, J. M. de Rutte, C.-Y. Wu, D. Di Carlo, and B. Ganapathysubramanian, "Flowsculpt: software for efficient design of inertial flow sculpting devices," *Lab Chip*, vol. 19, pp. 3277–3291, 2019. [Online]. Available: http://dx.doi.org/10.1039/C9LC00658C

[25] M. Antognoli, D. Stoecklein, C. Galletti, E. Brunazzi, and D. Di Carlo, "Optimized design of obstacle sequences for microfluidic mixing in an inertial regime," *Lab Chip*, pp. –, 2021. [Online]. Available: http://dx.doi.org/10.1039/D1LC00483B

[26] X. Y. Lee, A. Balu, D. Stoecklein, B. Ganapathysubramanian, and S. Sarkar, "A Case Study of Deep Reinforcement Learning for Engineering Design: Application to Microfluidic Devices for Flow



(a)



(b)

Fig. 14: Inlet pressure vs. capture efficiency for the Pareto Fronts for capture designs using different post shapes with up to 100 posts and totalling **(a)** 2000 designs and **(b)** 4000 designs. 0-25 Pa data is also magnified for better visualization for comparison. The results show that circular posts is overall best in attaining lower inlet pressure and higher capture efficiency. Square and pinwheel posts are the only posts able to attain 100% capture efficiency but with extremely high inlet pressures.

Sculpting," *Journal of Mechanical Design*, vol. 141, no. 11, 09 2019, 111401. [Online]. Available: https://doi.org/10.1115/1.4044397

[27] W. Ji, T. Ho, J. Wang, and H. Yao, "Microfluidic design for concentration gradient generation using artificial neural network," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 39, no. 10, pp. 2544–2557, 2020. [Online]. Available: https://doi.org/10.1109/TCAD.2019.2944588

[28] A. Lashkaripour, C. Rodriguez, N. Mehdipour, R. Mardian, D. McIntyre, L. Ortiz, J. Campbell, and D. Densmore, "Machine learning enables design automation of microfluidic flow-focusing droplet generation," *Nature Communications*, vol. 12, no. 25, pp. 2041–1723, 2021. [Online]. Available: https://doi.org/10.1038/s41467-020-20284-z

[29] Y. Hsieh and T. Ho, "Automated physical design of microchip-based capillary electrophoresis systems," in *VLSI Design 2011: 24th International Conference on VLSI Design, IIT Madras, Chennai, India, 2-7 January 2011*. IEEE Computer Society, 2011, pp. 165–170. [Online]. Available: https://doi.org/10.1109/VLSID.2011.47

[30] J. Potter, W. H. Grover, and P. Brisk, "Design automation for paper microfluidics with passive flow substrates," in *Proceedings of the on Great Lakes Symposium on VLSI 2017, Banff, AB, Canada, May 10-12, 2017*, L. Behjat, J. Han, M. N. Velev, and D. Chen, Eds. ACM, 2017, pp. 215–220. [Online]. Available: https://doi.org/10.1145/3060403.3060476

[31] ——, "Dynamic radial placement and routing in paper microfluidics," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 40, no. 10, pp. 1971–1984, 2021. [Online]. Available: https://doi.org/10.1109/TCAD.2020.3036836

[32] J. Potter, P. Brisk, and W. H. Grover, "Rapid development and optimization of paper microfluidic designs using software automation," *Analytica Chimica Acta*, vol. 1184, p. 338985, 2021. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0003267021008114

[33] M. Ibrahim and K. Chakrabarty, "Cyber-physical digital-microfluidic biochips: Bridging the gap between microfluidics and microbiology," *Proc. IEEE*, vol. 106, no. 9, pp. 1717–1743, 2018. [Online]. Available: https://doi.org/10.1109/JPROC.2017.2759251

[34] Z. Zhong, Z. Li, K. Chakrabarty, T. Ho, and C. Lee, "Micro-electrode-dot-array digital microfluidic biochips: Technology, design automation, and test techniques," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 2, pp. 292–313, 2019. [Online]. Available: https://doi.org/10.1109/TBCAS.2018.2886952

[35] V. Shukla, F. A. Hussin, N. H. Hamid, N. B. Z. Ali, and K. Chakrabarty, "Offline error detection in meda-based digital microfluidic biochips using oscillation-based testing methodology," *J. Electron. Test.*, vol. 33, no. 5, pp. 621–635, 2017. [Online]. Available: https://doi.org/10.1007/s10836-017-5678-5

[36] A. Grimmer, W. Haselmayr, A. Springer, and R. Wille, "Design of application-specific architectures for networked labs-on-chips," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 37, no. 1, pp. 193–202, 2018. [Online]. Available: https://doi.org/10.1109/TCAD.2017.2702562

[37] A. Grimmer, W. Haselmayr, and R. Wille, "Automated dimensioning of networked labs-on-chip," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 38, no. 7, pp. 1216–1225, 2019. [Online]. Available: https://doi.org/10.1109/TCAD.2018.2834402

[38] G. Fink, A. Grimmer, M. Hamidovic, W. Haselmayr, and R. Wille, "Robustness analysis for droplet-based microfluidic networks," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 39, no. 10, pp. 2696–2707, 2020. [Online]. Available: https://doi.org/10.1109/TCAD.2019.2962777

[39] A. Grimmer, W. Haselmayr, and R. Wille, "Automatic droplet sequence generation for microfluidic networks with passive droplet routing," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 39, no. 2, pp. 387–396, 2020. [Online]. Available: https://doi.org/10.1109/TCAD.2018.2887055

[40] G. Fink, M. Hamidovic, W. Haselmayr, and R. Wille, "Automatic design of droplet-based microfluidic ring networks," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 40, no. 2, pp. 339–349, 2021. [Online]. Available: https://doi.org/10.1109/TCAD.2020.2997000

[41] A. Grimmer, M. Hamidovic, W. Haselmayr, and R. Wille, "Advanced simulation of droplet microfluidics," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 15, no. 3, pp. 26:1–26:16, 2019. [Online]. Available: https://doi.org/10.1145/3313867

[42] G. Fink, P. Ebner, M. Hamidovic, W. Haselmayr, and R. Wille, "Accurate and efficient simulation of microfluidic networks," in *ASPDAC '21: 26th Asia and South Pacific Design Automation Conference, Tokyo, Japan, January 18-21, 2021*. ACM, 2021, pp. 85–90. [Online]. Available: https://doi.org/10.1145/3394885.3431608

[43] G. Fink, M. Hamidović, R. Wille, and W. Haselmayr, "Passive droplet control in two-dimensional microfluidic networks," *IEEE Transactions on Molecular, Biological and Multi-Scale Communications*, vol. 5, no. 3, pp. 189–206, 2019.

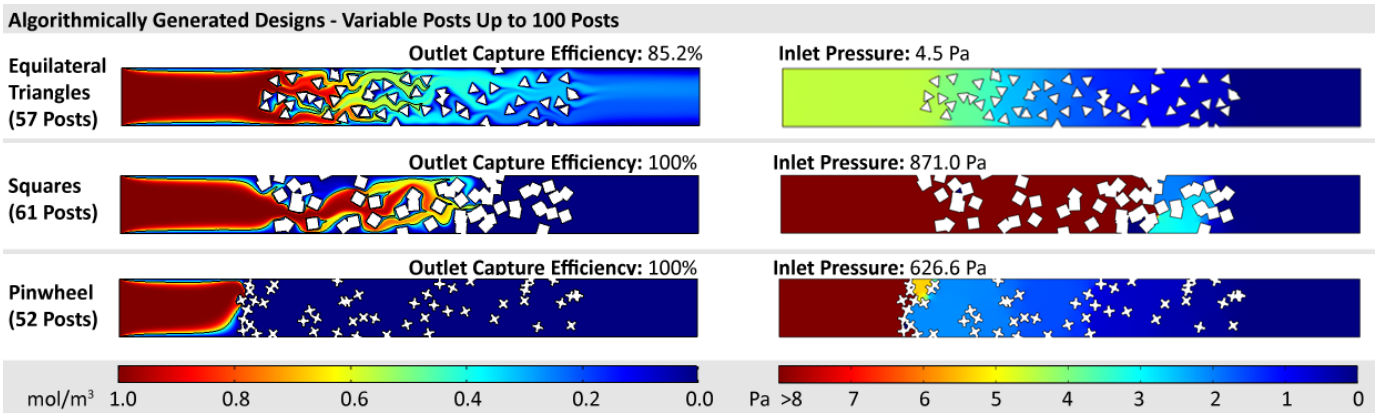


Fig. 15: Simulation results for the highest-capture efficiency chip designs for triangular, square, and pinwheel-shaped posts, discovered during the 4000 design runs reported in Figure 14b. **On the left** is the predicted concentration of capture target at each location of fluid in the chip during operation. **On the right** is the predicted pressure at each location of fluid in the chip during operation. Although the triangular posts performed best among the three new shapes in terms of achieve high capture effiency and low inlet pressure, the highest capture efficiency attained by triangular posts is still lower than the circular post design in Figure 13. Squares and pinwheels are able to obtain maximal capture efficiency, but the inlet pressures are likely to be too large for practical use.

Lisa Chen received the B.S. degree in Microbial Biology in 2010 from University of California, Berkeley. She worked in the medical devices and pharmaceutical industries for the next six years. She later obtained the M.S. degree in Computer Science from the University of California, Riverside. She is presently pursuing the Ph.D. degree in Computer Science from the University of California, Riverside.

Manu Sridharan is a Professor in the Department of Computer Science and Engineering at University of California, Riverside, working in the areas of programming languages and software engineering. He received his PhD from the University of California, Berkeley in 2007, and he previously worked at IBM Research, Samsung Research, and Uber. His research has drawn on, and contributed to, techniques in static analysis, dynamic analysis, and program synthesis, with applications to security, software quality, code refactoring, and software performance. His work has been incorporated into multiple commercial and open-source products, including IBM's commercial security analysis tool, the WALA open-source static analysis framework, and Uber's NullAway tool.

William H. Grover received the B.S. degree in chemistry from the University of Tennessee, Knoxville, TN, USA, in 1999, and the Ph.D. degree in chemistry from the University of California at Berkeley (UC Berkeley), Berkeley, CA, USA, in 2006.

He is an Associate Professor with the Department of Bioengineering, University of California at Riverside (UCR), Riverside, CA, USA. Prior to join- ing UCR, he received his postdoctoral training with the Biological Engineering Division, MassachusettsInstitute of Technology (MIT), Cambridge, MA, USA. In Prof. Scott Manalis' Group, MIT, he used the group's microfluidic mass sensors to make the first precision measurements of the density of single living cells. In Prof. Richard Mathies' Group, UC Berkeley, he developed microfluidic "processors" that bridged the chemical, biological, and computational sciences.

Philip Brisk (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in computer science from the University of California at Los Angeles, Los Angeles, CA, USA, in 2002, 2003, and 2006, respectively.

From 2006 to 2009, he was a Postdoctoral Scholar with the Processor Architecture Laboratory, School of Computer and Communication Sciences, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland. He is currently a Professor with the Department of Computer Science and Engineering, University of California at Riverside, Riverside, CA, USA. His current research interests include microfluidics, FPGAs, programming languages and compilers, and application-specific processors.

Prof. Brisk was a recipient of the Best Paper Award at CASES 2007. FPL 2009, and ReConFig 2019. He has been a Program Committee member for several conferences and workshops, including DAC, ASPDAC, DATE, VLSI-SoC, FPL, and FPT. He has been the General (Co)-Chair of the IEEE SIES 2009, the IEEE SASP 2010, and IWLS 2011, and the Program (Co)-Chair of the IEEE SASP 2011, IWLS 2012, ARC 2013, and FPL 2016. He is an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS and Integration: The VLSI Journal.